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CS548 Isolated Channel Oscilloscope System Specification

Summary

The CS548 is an individually isolated channel high CMRR oscilloscope with four channels. We can supply the unit with fewer channels – from none to three if that is all that is required. It is designed to measure all the signals in an operating full or three phase power electronic switching bridge on both the low and high sides. Examples include gate drives to measure voltage and charge, the power switch to measure loss and parasitic stress, the output to measure power and spectrum for EMC compliance, and the control system for Gain/Phase and stability. The CS5X8 includes an isolated signal generator for stimulus, and two expansion pod connectors for isolated input and output functions. Two CS548's can be slaved to make an 8 channel oscilloscope with coherent sampling. See the selected measurements at the end of the specification section for visual examples of measurements made. Other system components compliment the CS548 Oscilloscope and are summarized.

Front

Chan A - Chan D local and remote inputs:

- 2kVDC operating isolation voltage to ground and other channels. (Local)
- 30 kV operating isolation voltage to ground and other channels (Cat II), via CS1200 Remote Probe.
- 1 kVAC Cat III rating (local).
- 100 dB CMRR at 50 MHz
- 14 bit resolution, 100dB dynamic range
- 200 MHz Analog BW
- 20 pF to chassis
- Two hardware ranges:
  ±0.8V with 100uV resolution
  ±8V with 1mV resolution
- 200uV rms noise on 0.8V range
- probe isolators for protection.

Pod 1, 2 expansion

- 5 x Bidirectional 400 Mbps LVDS channels per pod.
- **CS1301** Isolated digital input pods included.
- **Optional Pods:**
  CS1302 Isolated four digital outputs + one input.
  See also **Further Pod development**
- **Pulse Builder** for Pulse Trains, PWM, and double pulse generation.

CS1200 Remote Probe

- Remote fibre connected digitizer head up to 30m from CS548.
- 2pF to ground.

Pulse generator/ Calibration

- Probe Comp output ~ 1ns rise, fall -time, programmable 5-12V level.
- Programmable Pulse train, PWM or double pulse.
- Programmable DC Cal output for complete probe and channel DC calibration. Ref is 7.5V or 0.6818V ± 0.035%, or short to ground.

Power Button

- Push On- Push Off power button.
- Rear 2 pin connector for remote power or power at start operation.

Back

Signal Generator:

- Isolated 600V working
- 0 - 65 MHz
- 14 pF to chassis
- 100 dB CMRR at 50 MHz
- Sine, square, arbitrary (incl patterns)* 100uV rms noise

Digital Port:

- 16 bi-directional pins connected to Silego SLG46826V analog/digital programmable device
- Trigger In/Out connection*

Link Port:

- Links to CS1070 0-50 MHz 1A power amplifier, CS1133 VSat probe.
- Includes Uart, SPI and I2C I/O*
- Trigger and control *

SD Card:

- Store stand-alone captures to the SD Card *

USB:

- USB 3-C socket
- USB3 @ 130MBps
- USB2 @ 30 MBps

Ethernet: *

- SFP socket based
- Copper 10/100/ 1000 Mbps
- Fibre 1Gbps

Triggering

- Two FPGA mixed signal triggers
- Triggers interpolate in time for higher trigger accuracy.
- Triggers may be combined using AND/OR/XOR
- Triggers may be sequences Trigger 1 [num occurrences] - time specification - Trigger 2 [num occurrences] . The time specification is less than a period, in a period range or more than a period. Triggers may be completely independent.
- The digital portion may be rising or falling digital input, conditional on one or more other digital inputs being 0, 1 or don't care. Bit's may be OR'd or AND'd.
- The analog trigger may be conditional on a digital state.

Power In:

- 10- 24V DC, 42W.
- Can be car power supply connected, withstands crank and load dump.

Link In/Out:

- Used to daisy chain multiple units
- Synchronous sample clock
- Trigger and control

CS548 Included Components

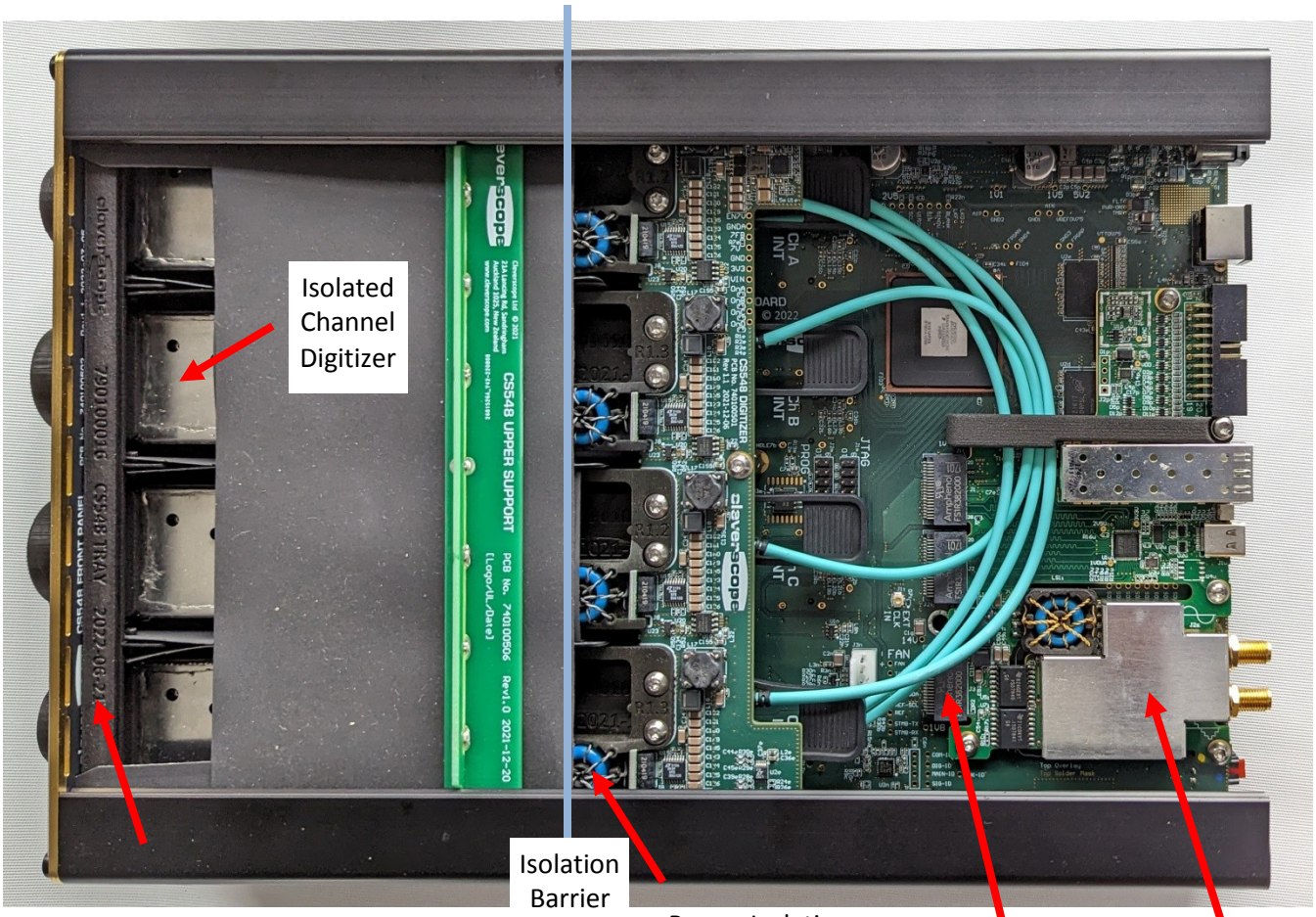
The CS548 includes 1 off 1x/10x probe, 100x probe and Common Mode Choke per installed channel, 2 off CS1301 Input Pods, USB Cable, Power Supply, SMA-BNC adaptor, Ethernet SFP module (copper or fibre).

* Item still to be implemented. See Specification Status section.

CS548 Channel Isolation

The CS548 digitizers are held in a plastic insulator tray to maximize creepage and clearance. The tray has a CTI>600, and conforms to Materials Group 1 in the IEC61010-2 standard. We build for use in Pollution Degree 2 environments (only non-conductive pollution occurs except that occasionally a temporary conductivity caused by condensation is expected). The CS548 is for use with up to Category III circuits (permanently connected to the mains switchboard via a fuse).

Each shielded channel digitizer is completely separate and attached to the digitizer power board using a spacer for high CMRR and isolation. The plastic / transformer former (CTI >600) provide a creepage >22mm and clearance > 18mm. The low capacitance transformers use triple insulated Rubadue wire (T32A01T5XX-1.5). The Active Optical Cable link to the Main board (500mm) has a breakdown voltage >30kV. Each channel is isolated from the chassis and other channels using high dielectric RS Pro 785-0809 (24kV BV, 600V CTI) plastic sheets.



We have built the CS548 with the assumption that the UUT is powered by a line to neutral mains voltage <600Vac, and includes secondary circuit working voltages of <2240 Vdc or acpk. This is measurement category III. These standards apply:

Clearance:

- IEC61010-1 (ed 3.0) Table K.11, Reinforced = 2 x 6.9mm = 13.8mm
- IEC61010-2-030 Ed 1.0 (Test Equipment), Table K.101, a reinforced insulation clearance: 10.5 mm.

We use 18mm.

Creepage:

IEC61010-1 (ed 3.0) Table K.13, 2000Vdc, Reinforced = 2 x 10mm = 20mm.
We use 22mm.

Warnings

The Isolated Analog Inputs **CHAN A..D** and **SIG GEN** outputs may have high common voltages applied to the coaxial connectors.

Do NOT touch any connectors connected to the Channels or Sig Gen during operation. Ensure all connected voltage sources are turned off before changing any connector. Verify this using a multimeter.

The **CHAN A..D** inputs are rated at a maximum of 2kV DC common mode to real earth, and 1kV signal to BNC common. **Do NOT exceed these values**.

The **SIG GEN** output is rated at 600V AC between the coaxial connector common and real earth. **Do NOT exceed this value**.

Do NOT allow liquids to enter the CS548.

Do NOT block the CS548 ventilation holes, including placing the CS548 upside down.

Do NOT exceed an input supply voltage of 30VDC.

Do NOT lick.

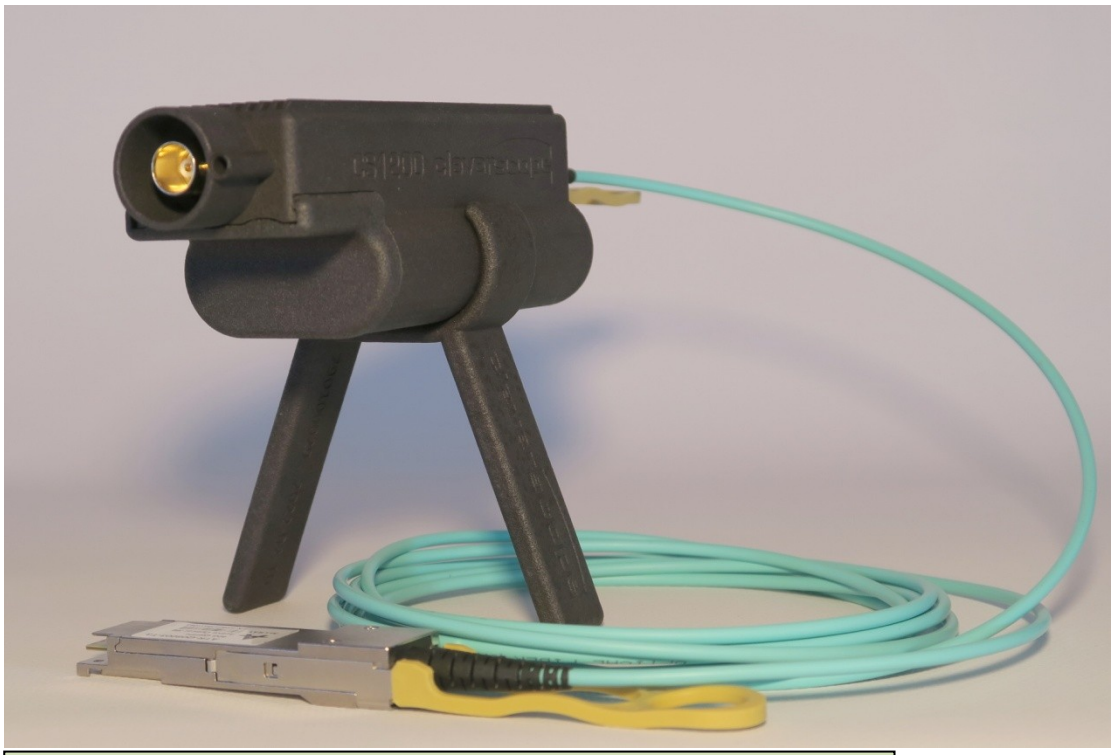
If the CS548 equipment is used in a manner not specified by Cleverscope, the protection provided by the equipment may be impaired. For example, safety will be impaired if exposed metal connectors are used.

If cleaning the CS548, use only a damp cloth to wipe down any surfaces. Do NOT use IPA or alcohol based products.

System Accessory Probes and Pods

CS1200 IsoPod

The CS1200 **IsoPod** is a remote isolated digitizer Pod for the CS548. It uses a standard QSFP terminated active optical cable (AOC) to connect the CS1200 IsoPod to the QSFP remote sockets on the CS548 front Panel. The input specification is identical to the CS548 internal channels. The CS1200 is an optional purchase.



CS1200 IsoPod

- 30kV isolation provided >150mm spacing between IsoPod and other structures.
- Pod enclosure isolation to BNC > 1kV
- 2 pF free space capacitance >50 mm above reference plane
- 100 dB CMRR at 50 MHz
- 14 bit resolution, 100dB dynamic range
- 200 MHz Analog BW
- Two hardware ranges:
  ±0.8V with 100uV resolution
  ±8V with 1mV resolution
- 1 M Ohm // 21 pF input impedance

The CS1200 allows time aligned measurements to be made between locations up to 60m apart (using 30m cables), and measurements in hazardous, high voltage situations. The Isopod batteries are standard 21700 5AHr cells, and offer more than 8 hours operation before recharge. One set of cells can be recharged while the other set is being used.

It is assumed that the CS1200 will be used with the standard oscilloscope probes supplied with the CS548. However, short attenuating probe tips are available. These allow operation in high common mode slew applications with a minimum of common mode artifacts.

The standard Active Optical Cable length is 3m. Lengths of 5, 10, 30m are available on request.

CS1133 V_{SAT} Probe

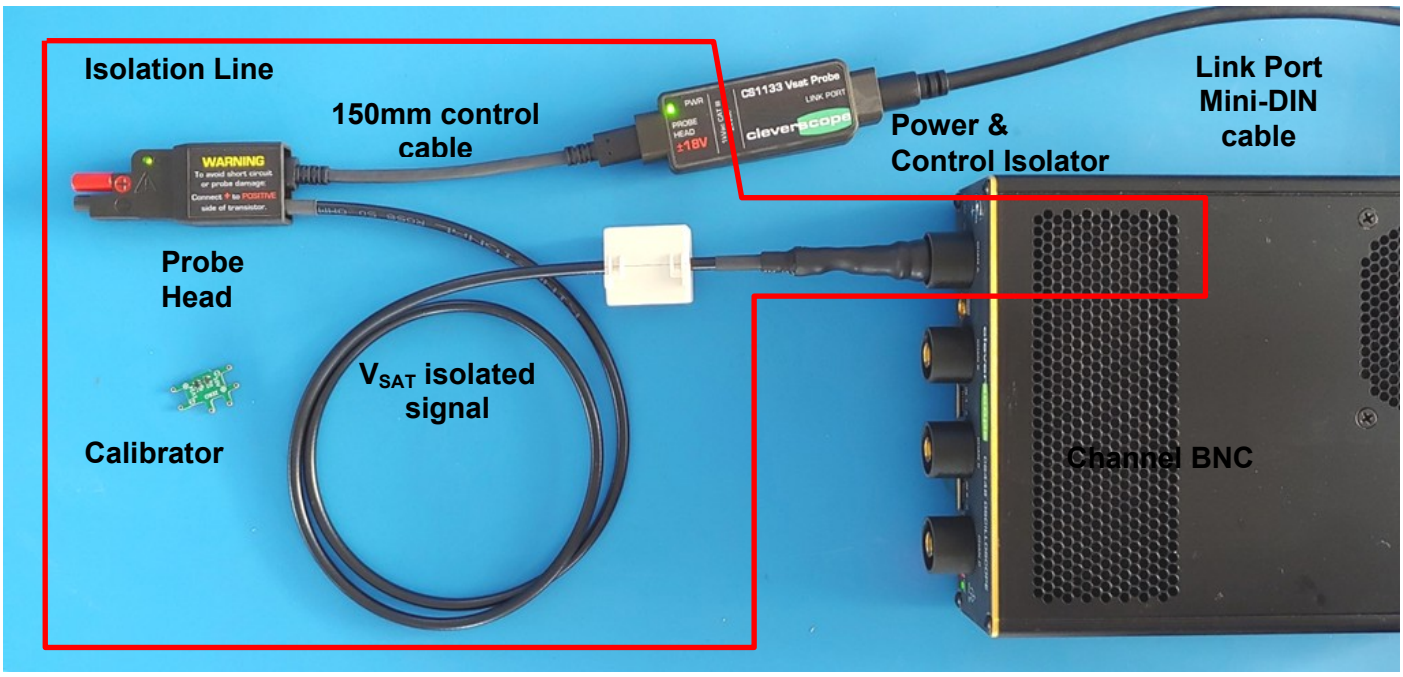
The CS1133 **VSAT probe** is used to measure the saturation voltage of a switching transistor. It uses a 30mA high compliance current source to measure the transistor forward voltage while the voltage across the device is less than the clip level. The clip level can be set to 3 ranges; approximately 15V, 1.5V and 150mV. Above the clip level the VSAT probe is disconnected from the Unit Under Test (UUT). It is expected that the UUT will have a good deal more than 30mA flowing through it so this small additional current will not significantly change the saturation voltage. The CS1133 is designed to work into a 50 ohm load. The CS1133 is rated for operation over the input voltage range of 0V to +3.3kV. It can also withstand negative overshoot on the UUT down to -100V for short term transients.

The CS1133 is powered by +5V sourced by the CS548 LINK PORT (pin 1) and 0V (pin 2) via an 8 pin Mini Din Connector. It also includes two controls to select clip level; IN1 (pin 8) & IN2 (pin 5). The power and control signals are isolated via a low capacitance isolated power supply and optical isolators housed in a separate unit. The maximum working isolation voltage is 1kVAC CAT III or 2kVDC. In addition the active portion of the CS1133 is shielded to ensure it can be used to measure the high side transistor while it is switching.

The CS1133 is an optional purchase.

System Isolation

When used with the input channel isolation of the CS548 the CS1133 can be used to measure V_{SAT} of a high side or floating transistor. This diagram shows where the isolation occurs



All items within the isolation line (Channel A, Probe Head, Coax cable and output of Isolator) have a common reference connection which will be connected to the UUT Source (or Emitter). If the Source is a high side transistor in a half bridge this whole isolation island will move with the switching edges of the half bridge. A common mode choke (as supplied with the CS548) may be required on the coax cable to suppress common mode induced LC ringing between the coax outer inductance and the measurement point capacitance.

CS1133 V_{SAT} Probe

- +3.3kV maximum VDS
- 50 ns recovery time (1kV falling edge)
- 2kV DC working isolation voltage (1kV AC CAT III)
- Clip Levels: 15V, 1.5V and 150mV
- Gain Accuracy < ± 1%

CS1300 Series Pods

The CS1300 Pods are used to extend the capability of the CS548 oscilloscope. Two Pod connectors are provided on the CS548. Pods use LVDS communications capable of 400 Mbps for good noise immunity, low EMI, and reliability. These pods are available now:

1. **CS1301 Isolated digital inputs.**
   Two CS1301 pods are included with the CS548.
   The pod supports 4 isolated digital inputs with one common, and fixed voltage threshold of Vhi > 2.3V, with +18, -15V overload protection.

   Isolation is 600V RMS Cat III (UL), or 800 DC (VDE), based on an ISOW7844FDWE, and PCB creepage. Common mode rejection is 100V/ns.

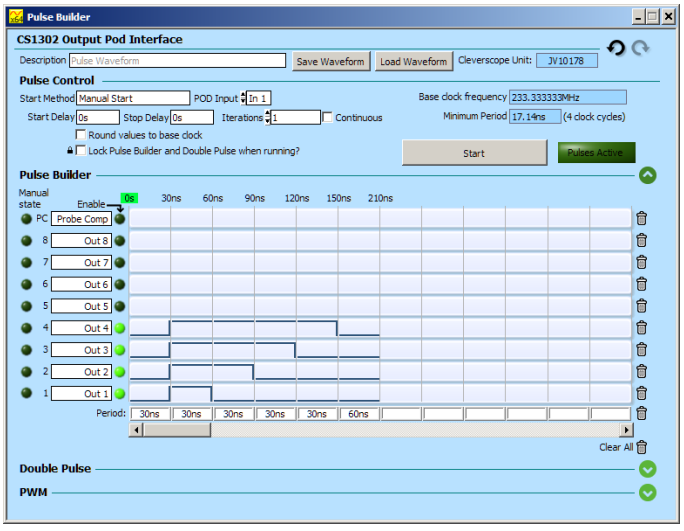
2. **CS1302 Isolated digital outputs.**
   The CS1302 is an optional purchase.
   The pod has 1 input, and 4 outputs, one of which may be assigned as a high speed clock. The pod allows high speed generation of arbitrary signals, optionally synched to the clock, with simultaneously recording of the input signal. It may also be used as a fast isolated SPI or UART port. The application supports arbitrary pulse generation, PWM, and double pulse testing using the CS1302.

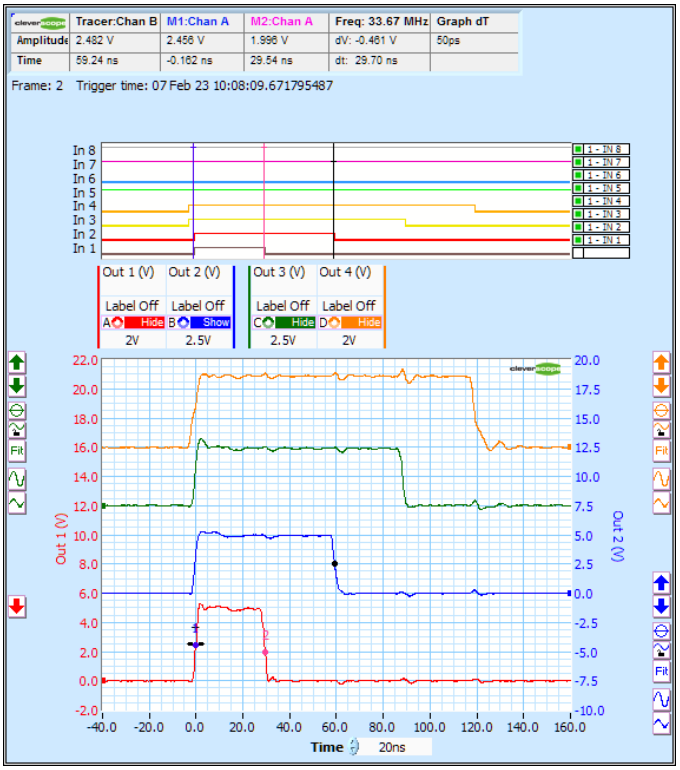
   The output level is 5V (V_{SEL} open), or 3V3 (V_{SEL} pulled low).

   Isolation is 600V RMS Cat III (UL), or 800 DC (VDE), based on an ISO7840DW and ISOW7744DFMR, and PCB creepage. Common mode rejection is 100V/ns.

Pulse Builder

The CS1302 is supported by Pulse Builder in the Cleverscope4 application. Pulse Builder can be used to draw pulse trains, Double Pulse Test pulses, and PWM output with arbitrary durations between each edge:



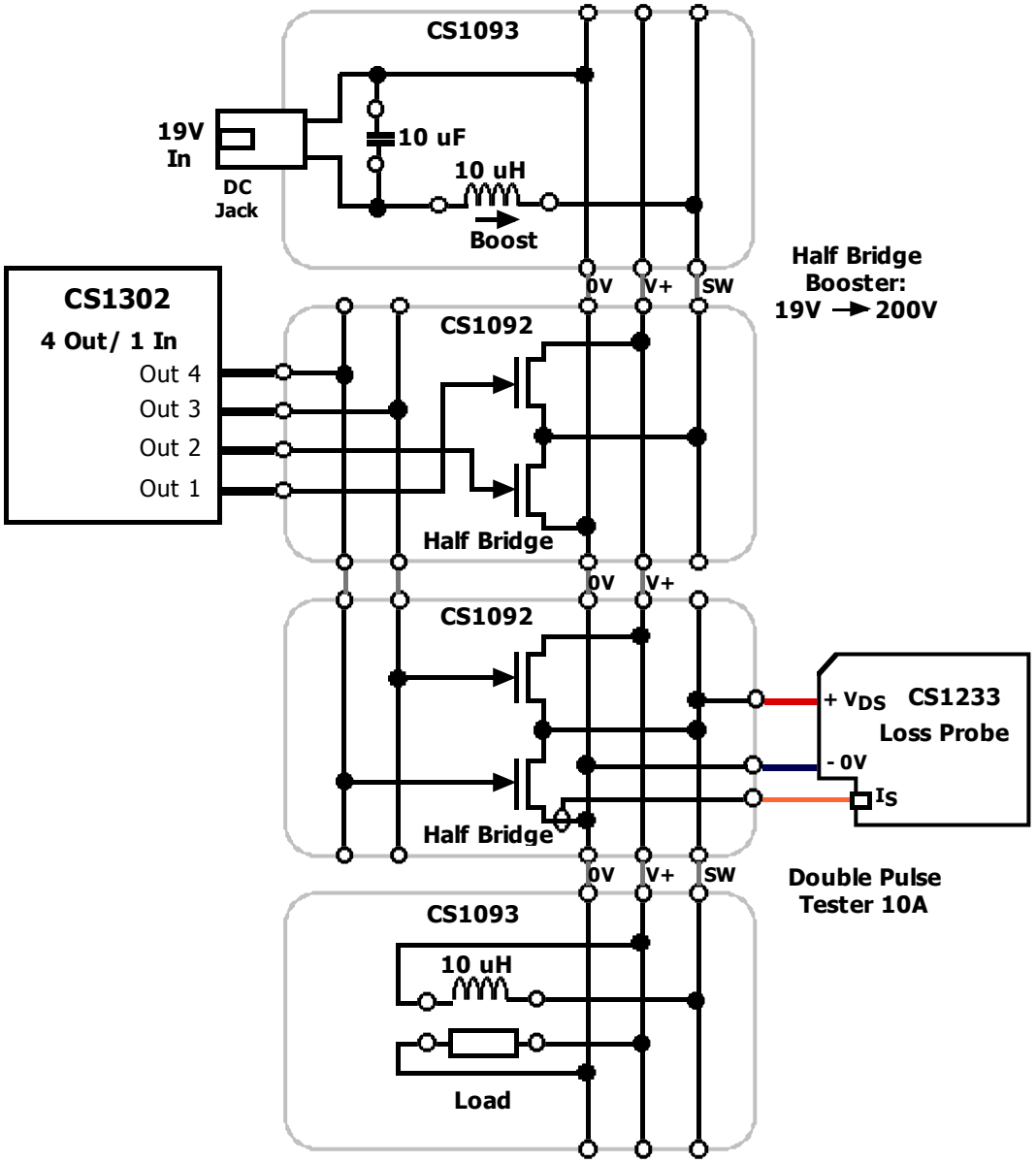


Here 4 pulses have been defined, and output via a CS1302. Outputs 1-3 are mirrored as Inputs 1-3. Input 4, which is a CS1302 input, is physically measuring Output 4. Pulses as short as 17ns can be generated using the CS1302. These pulses are 30, 60, 90 and 120ns long.

CS1092 GaN Half Bridge, CS1093 Half Bridge Load Experimentation Modules

Cleverscope has developed three credit card sized modules to aid in applying and proving design ideas for power electronic topologies. The modules are the **CS1092** GaN Half Bridge, the **CS1093** Half Bridge Load, and the **CS1094** Current Pulser. They stack together using a control line bus on the left, and a power and switch bus on the right.

Concept Diagram for a Double Pulse Tester Operation



The CS1093 is configured as a boost converter. The 10uH inductor is used to increase the voltage from 19V to 200V

The CS1092 SW terminal uses PWM on the lower transistor to boost the voltage to 200V. The high side free wheel diode routes current to V+

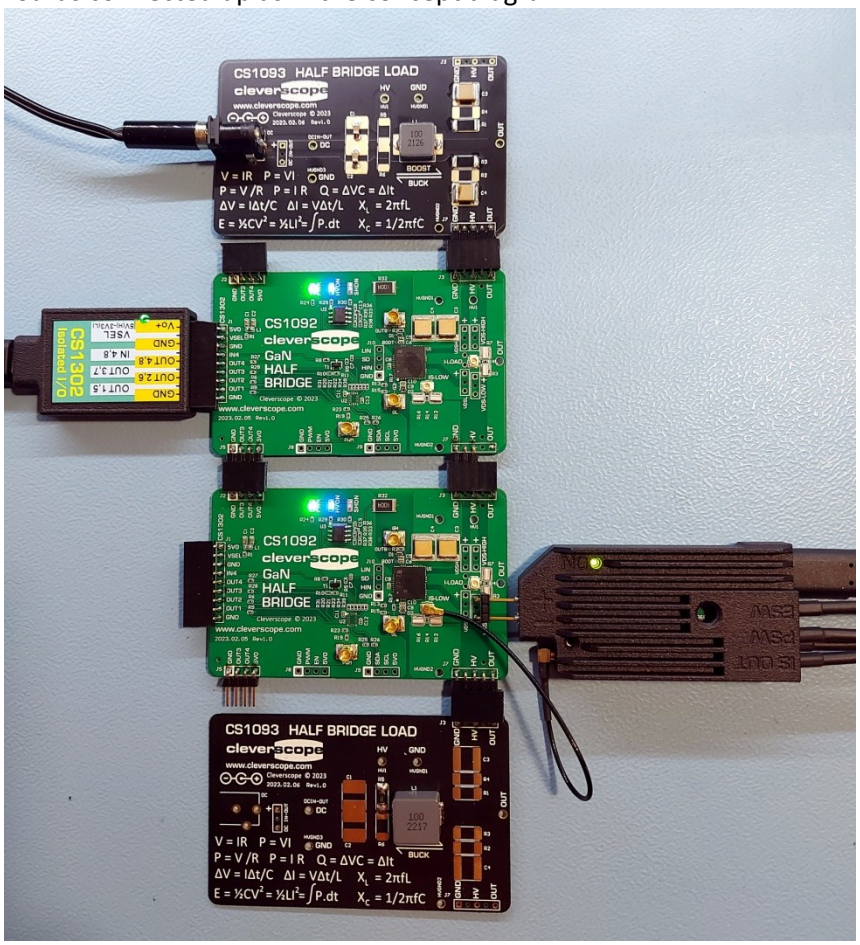
The CS1092 acts a double pulse tester, with the low side transistor switching the load inductor to V+ to allow the double pulse ramp.

The CS1093 is configured as a 10uH load inductor. A resistive load stabilizes the V+ bus.

The devices in the CS1092 allow safe operation to 200V and 10A. The half bridge driver is a ST MasterGAN1, rated for 520V, 9.7A operation (at 25 deg C). Rds is 150 mOhm. This is sufficient for the evaluation.

The CS1302 provides the PWM controls for the booster (using Out 1 and 2), and the Double Pulse control (using Out 3 and Out 4). Input 4 is wired to the MasterGAN1 over temperature output (not shown here).

Boards connected up as in the concept diagram



CS1093 Half bridge Load

CS1092 GaN Half bridge

CS1302 4 Out +1 In Pod

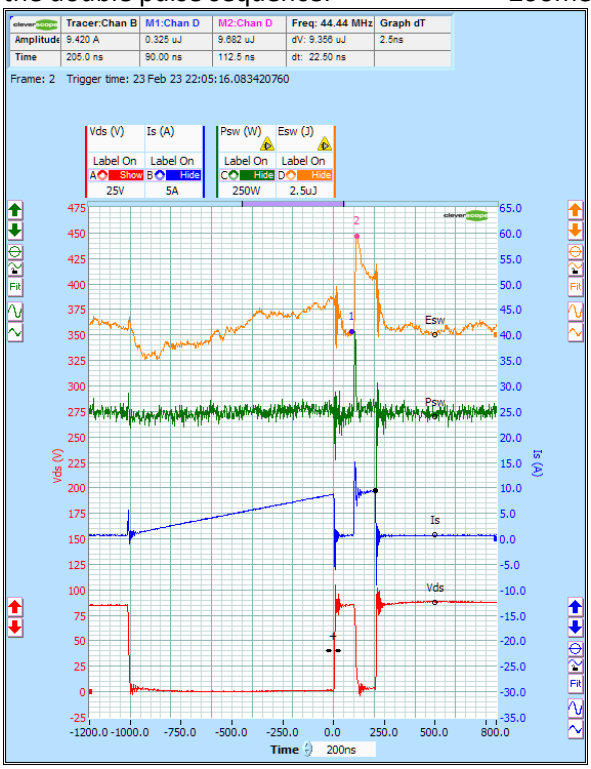
CS1092 GaN Half bridge

CS1233 Power Probe

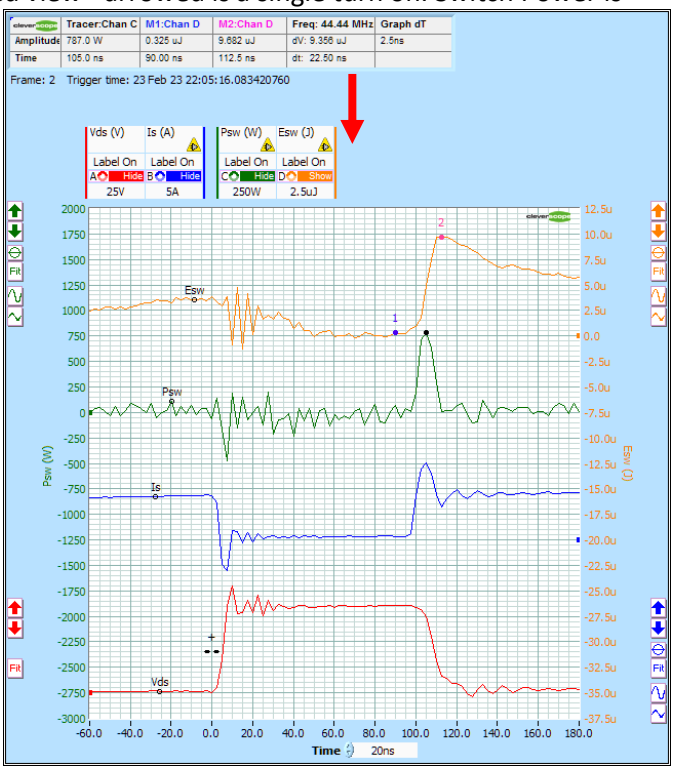
CS1093 Half bridge Load

Below are waveform recorded using this arrangement. The Bus voltage is about 85V, and the maximum current about 9.4A. Psw is the instanatenous power, and Esw the integrated energy. By measuring differences between two points on the graph we can measure the Power for that event. Markers 1 and 2 are used for this.

This is the double pulse sequence:



Zoomed view - arrowed is a single turn on. Switch Power is 9.4uJ.



Further Pod Development

Cleverscope has these pods in or planned for development:

1. **CS1303 Isolated Current Measurement**
   This pod will use 4 x TI AMC3306M05 with ±50mV input range, to provide 4 individually isolated channels for current sense (50mV current sense resistor such as Murata 3020 DMS shunts). The CS1303 can measure three phase currents and a bus current.
2. **CS1304 Isolated Voltage Measurement**
   This pod will use 4 x TI AMC3336 with ±1V input range to provide 4 individually isolated channels, for voltage sense. A voltage divider plugin will be provided to cover up to 2kV. The CS1304 can measure three phase voltages, and one bus voltage. The application will be upgraded to include a power analysis function to measure power, harmonic structure, power factor, and efficiency.
3. **CS1305 Log Pod.**
   For logging of slow signals on the Signal Information Logging Screen. Uses an AD7124-8 8ch 24bit SPI ADC. Can be used to log 4 channels of temperature (using an RTD) and 4 channels of voltage measurement, or 4 channels of thermocouple with RTD based cold junction temperature compensation (see Analog Devices CN-0391). So this pod can be used to measure such things as a device with ambient, internal and 2 hot spot temperatures and PSU voltages and current. Or a battery charge/discharge cycle monitoring voltage, current and temperature. If using thermocouples very high temperature measurement is possible. The logging system runs separate from the capture system so that logs can run continuously, independent of trigger.
4. **CS1306 CAN controller**
   The CAN controller will use an SPI CAN controller (such as Microchip MCP2515 or TI TCAN4550) to monitor or stimulate CAN messages in an automotive CAN network.

Analog Inputs

* Item still to be implemented. See Specification Status section.

Parameter	Specification	Notes
Number of channels	0 - 4	Fibre optic isolated from each other, local or IsoPod.
Isolation Voltage - Local	2kVdc Cat III, when connected to mains systems of less than 600V line-neutral	Supported by IEC 61010-1 Ed 3.0 and IEC 61010-2-30 (Test Equipment) 22mm creepage and 18 mm clearance, reinforced, Category III. Plan to certify to CE
Isolation Voltage –Remote IsoPod	±30 kVdc	When mounted >150mm from reference plane or other structures not at the common mode voltage. If measured signal frequency is >1 MHz, then must be mounted >1m from any other conductive structure not at the common mode voltage.
CMRR	> 120 dB at 1 MHz > 115 dB at 10 MHz > 100 dB at 50 MHz	20dBV signal applied to coax common and earth reference 4mm socket.
ADC resolution	14 bits	
Input Ranges	±0.8V with 100uV resolution ±8V with 1mV resolution	Use probes to extend the range, eg 800V with 100x probe. The application automatically scales all values to compensate for probe attenuation.
DC voltage measurement accuracy	<±0.15% of range maximum.	After self calibration or calibration.
Sample Rate	500 MSPS * 400 MSPS now	All Analog and Digital channels simultaneously.
Sample Memory	500 M Samples * (installed)	Currently 4 x simultaneous channels with 10M per channel.
CM leakage to other channels	<-125dBc	20 dBV signal to CM channel, measured on other channels whole bandwidth, ±0.8V range
Channel to Channel Skew	< ±144ps	Done using a 1 MHz coherent sine wave
Cross talk at 10.7 and 30 MHz	< -115 dBc	Using 1.6V p-p into the channel
RMS Channel Noise 1 M samples	~ 200 uV rms, ±0.8V range ~ 2mv rms, ±8V range	Inputs open
Pk-Pk Channel noise 1 M samples	1.8mVp-p for ±0.8V range 15mVp-p for ±8V range	Inputs open
Sample clock jitter	300 fs rms	
Sample clock Freq tolerance	max ±2ppm	At 25 deg C
Sample clock temp stability	max ±0.5 ppm	Over -40 to +85 deg C
Enob (rms)	11.6 bits, or 1 part in 3,300	Inputs open
Noise free bits	10.3 bits, or 1 part in 1300	Inputs open
Spectral Noise floor, no protrusions	-100 dBV -115dBV	<2MHz, 200 MHz BW, 1kHz resolution >2MHz, 200 MHz BW, 1kHz resolution
Sinad	> 64 dBc at 1 MHz > 63 dBc at 10 MHz > 55 dBc at 30 MHz	1 Vp-p into 50 ohms signal
HD2+3	< -80dB at 1MHz < -76 dB at 10 MHz < -71 dB at 30 MHz	1 Vp-p into 50 ohms signal
THD	< -76 dB at 1 MHz < -74 dB at 10 MHz < -67 dB at 30 MHz	1 Vp-p into 50 ohms signal
Pulse Flatness	< 700uV < 2mV < 200mV	0.5V pulse, 500us duration, ±0.8V range 0.5V pulse, 500 us duration, ±8V range 500V pulse, 500us duration, 100x probe
Overload recovery	4ns	Recovery from 10x overload
Maximum Differential Input Voltage	±1 kV, derated above 1 MHz.	Derated at 20dB/decade
Maximum Common Mode Input Voltage	±2 kV, derated above 10 MHz.	Derated at 20dB/decade
Spectral Flatness	±0.5dB from 0 - 160 MHz -3 dB at 200 MHz	Supports 200 MHz Bandwidth
Input Resistance	1 M Ohm	DC resistance
Input Capacitance	22.0 pF	Signal Input to Signal Common
Isolation Capacitance	20 pF	Channel ground to chassis

Digital Inputs

Parameter	Specification	Notes
Number of inputs	8	
Common mode transient immunity	100V/ns	
Input threshold max	2.3V rising 0.9V falling	Using CS1301 isolated probes (ISOW7844). Using CS1300 threshold programmable 0-8V.
Isolation capacitance	< 5pF	To chassis ground, at 1 MHz
Isolation operating voltage	880V DC (600 VAC rms) 1130V DC	Re-inforced insulation, EN61010-1 Re-inforced insulation, CSA and IEC 60950-1
Maximum Data rate	100 Mbps	Sampled at 500 MSPS* (400 MSPS now).
Propagation delay	13ns typ	Compensated for within CS548

Signal Generator

Parameter	Specification	Notes
Output Frequency Range	DC - 65 MHz	-3dB at 65MHz on un filtered output
Outputs	Unfiltered, filtered	Unfiltered is used high slew rate signals (AWB or square wave). Filtered includes a reconstruction filter for minimum sample clock injection into the signal.
CMRR	> 100 dB at 1 MHz > 95 dB at 10 MHz > 90 dB at 50 MHz	Limited by analog channels used for test. The Sig Gen connection reduces CMRR by about 20 dB, if direct connected to a Channel.
Common mode transient immunity	100 kV/us	For control of the output DAC
Isolation Voltage	880 VDC (600VAC rms working)	Supported by IEC 61010-1 creepage and clearance, reinforced, Category III Plan to certify
Unfiltered rise/fall time	3.2ns	Full scale swing
Sine Wave Flatness	±0.2 dB +0.2 -3 dB	0 - 20 MHz filtered + unfiltered, 50 Ohm terminated 20 - 65 MHz unfiltered
DAC resolution	12 bits	
NCO Resolution	24 bits	10.7 Hz resolution at 180 MSPS
Output amplitude	±1mV to ±3.5V p-p	Programmable 1mV resolution, constrained to total range ±3.5V including offset
Output offset	0 to ±3.5V p-p	Programmable, 1mV resolution
Output Noise	< 100uV rms	
SFDR	> 84 dBc	At 10 MHz
IMD	> 88 dBc	At 10 MHz
HD2+3	< -77dBc	At 10 MHz
Arb Waveform Memory	4 k Samples *	Using AD9102 - UI to be implemented still
Sample Rate	180 Msps	Programmable Sample rate 1sps - 180 Msps
Frequency list values	2k *	Frequency list output in response to trigger
Envelope can be amplitude modulated	Yes *	
Pattern Generator	Yes *	Start period, output period, stop period, pattern repeat count.
Trigger	Input from FPGA *	FPGA may trigger a pattern based on Channel Trigger or other event.

USB

Parameter	Specification	Notes
Supported Modes	USB 2.0 and USB 3.0	USB 2.0 @480 Mbit/sec and USB 3.0 at 5 Gbps
Throughput	30 MBps and 130 MBps	
Connector	USB-C	Plug is reversible
Protection	Common mode choke + ESD diodes	Using ECMF04-4HSWM10
Indicators	USB on and correctly connected	Power of signal is indicated by LED off.

Ethernet *

Parameter	Specification	Notes
Connection method	Small Form factor Pluggable module (SFP)	An SFP socket is provided for use with an SFP module. Either an optical or a copper connected SFP module will be supplied based on the order.
Wired Supported Modes	Ethernet 10/100/1000 *	Using an RJ45 Ethernet socket connected copper SFP module. Transformer based isolation.  Software being implemented
Optical supported mode	Ethernet 1000BASE-LX *	Gigabit (1G) Ethernet using an LC fibre cable connected optical module. Full optical isolation.  Software being implemented
Throughput	12 MBps and 120 MBps	
Connector	SFP Socket	Small Form Factor Pluggable socket
Indicators	Ethernet on and correctly connected	Power of signal is indicated by LED off.

Power Supply

Parameter	Specification	Notes
Input Voltage Range	10-24 DC	Over voltage protected
Power consumption	42W	
Connector	Barrel Socket, 2.5mm I.D. x 5.5mm O.D	Connection is reverse polarity protected.
Protection	Clamped to +68V Clamped to -32V Operates with 35V Survives with 5V	ISO16750 pulse A (79 ohm 0.5 ohm) ISO7637 Pulse 1 (-600V, 50 ohm) FPGA operation at 5V, ADC operational at 7V.
Indicators	Power On, Channel Status	Software controlled.

Digital Port *

The Digital Port is based on a programmable logic IC, and can be used for generating complex state based sequences or reacting to a complex set of inputs. The port includes triggering capability. The UI has not been completed.

Parameter	Specification	Notes
Input/Outputs	16	Programmable as In or Out
Logic Level	Programmable 1.8 - 5V	All I/O operate at the same logic level
Control IC	Silego SLG46826V	User configurable programmable logic with analog functions
Resources	19 Multi-function Macrocells Prog Oscillator, 25MHz, 2MHz, and 2 kHz. 256x8 EEPROM 4 Analog Comparators 2 x Deglitch filters Two voltage references I2C port	2-4 bit for complex logic All resources can be arbitrarily connected as required.
Programming	Silego GP Designer	Visual schematic designer of circuit functions downloaded into CS548
Trigger In/Out	Bidirectional Trigger	For interaction with measurement system.
Protection		Over voltage protection to +12V and -6V

Link Port *

The Link Port is used for controlling Cleverscope accessory devices such as the CS1070 1A 50 MHz power amplifier, and the CS1110 V_{CE} Sat Probe. It also includes RS232, SPI and I^2C ports for controlling user equipment.

Parameter	Specification	Notes
Digital Port Use	2 Digital In, 4 Digital Out	Used for accessory control
I2C Port	400 pbps port	For control of user devices
SPI Port	1 MHz SPI Port	For control of user device, mutually exclusive with RS232 Port
RS232/RS422 Port	3V level RS232 port, or differential RS422 port, programmable baud rate	For control of user device, mutually exclusive with SPI Port
Trigger Port	Trigger In/Out and control	Used for linkage to CS328A link port
Protection		Over voltage and reverse voltage protection using ESD devices

Link In/Out Port

The Link In/Out Port is used daisy chaining 2,3 or 4 CS548 Cleverscopes.

Parameter	Specification	Notes
Clock ports	Reference clock, 500 kHz	The last CS548 in the chain provides the 500 kHz reference clock that is used for simultaneous sampling by all units.
Trigger Ports	Trigger transfer	The Trigger Ports transfer the triggering unit's trigger to other units.
Control Ports	Control signals	The control signals are used to signal readiness to trigger, and sampling state.

See the selected measurements section for an example 8 channel display.

Probe Compensator Output

The probe Compensator output is used to compensate the probe response for time domain flatness.

Parameter	Specification	Notes
Signal	1 kHz Square Wave	Variable 50mHz to 58.3 Mhz
Duty Cycle	50%	Variable with 8.6ns resolution to 10s high.
Amplitude	Programmable 5-12V	
Rise/ Fall Time	~ 1ns	
Connection	BNC, 50 Ohm source	Designed for 10x probe. 10mV dip with 50 Ohm load.

Environmental

Parameter	Specification	Notes
Temperature	0°C to +40°C -20°C to +60°C	Operating Storage
Cooling Method	Fan Assisted	
Humidity	0°C to +40°C >40°C	<90% relative humidity <60% relative humidity
Altitude	<3,000m 15,000m	Operating Non-operating

Mechanical

Parameter	Specification	Notes
Size	Height 69 mm Width 187 mm Length 280 mm	Including feet Including connectors
Weight (approx)	2.8 kg 4.1 kg	Acquisition Unit only Complete in display box
Material	Anodized Aluminium	

Specification Status

The CS548 is FPGA based, and upgradeable in the field. The customer can use Cleverscope Rom Loader to download new firmware and logicware to improve or add functions to the unit. The hardware system for the CS548 has been thoroughly tested to meet the specifications above, and includes all the resources needed to meet the full specification. However some software functions are still to be added. As these are added, updates are placed on our website for download at no cost. Cleverscope has used this method for years to add features such as FRA, streaming, complex maths etc. Should the current specification set meet your needs, you are able to use the CS548 now, and upgrade, at no cost, as further functionality becomes available.

Key features that still have to be implemented are:

Feature	Specification	Note
Sampling Rate	500 MSPS	Currently the sample rate is 400 MSPS. It will be upgraded to 500 MSPS on the completion of the Ethernet system.
I/O Interfaces	Ethernet is supported	Ethernet is currently not supported. We have implemented a hardware based IP stack, which is functional. Integration is proceeding with the CS548 firmware.
Sample Memory	250 MSamples.	Physical memory for 500 MSamples (16 bit) is provided. Currently we use only 40 MSamples of it organized as 4 fixed simultaneous buffers of 10MSamples - one for each channel. We will provide options of 500 MSamples/1 channel, 250 MSamples/2 channels and 125 Msamples/4 channels in the future once the application allows.
Two unit Linking	Two unit linking via Link In and Link Out Ports	Two units linking is functional. An example is given in the selected measurements. We do intend to allow up to 4 units to link, but some work still needs to be done for this.
Signal Generator Waveforms	The signal generator will support AWB	The isolated Signal Generator currently only supports Sine and variable duty cycle Square wave generation and sweeping. The hardware (based on the AD9102) can generate 4K Arbitrary Waveforms, and patterns. The sig gen design includes a swept clock source to allow sweeping arbitrary waveforms (including square and triangle waves). The user interface for this is not yet done.
Link Port	The Link includes SPI, UART and I2C generation	The Link Port includes the facilities to generate I2C, Uart and SPI messages, as well as digital outputs. This capability is already supported by the firmware and DLL driver. However a UI has not been implemented in the application. This will be done as time permits.
Real time Sample Filtering	Real Time sample filters to improve dynamic rang	The filter block for the programmable FIR filter has been implemented, but is operating with a fixed coefficient set. The firmware to load a variable coefficient set still need to be implemented.
Faster Peak Capture	Replay Peak Capture to run at close to real time	The current system has real time peak capture where the decimator outputs samples at below the maximum sample rate (eg Streaming). However, the replay peak capture system, while working, is not optimized and relatively slow. A DMA/Hardware based system will be used for peak capture replay.
Digital Port	Full use of Silego SLG46826V	Hardware has been tested. The Silego programmer can be used. The CS548 will provide Silego design download at some point.

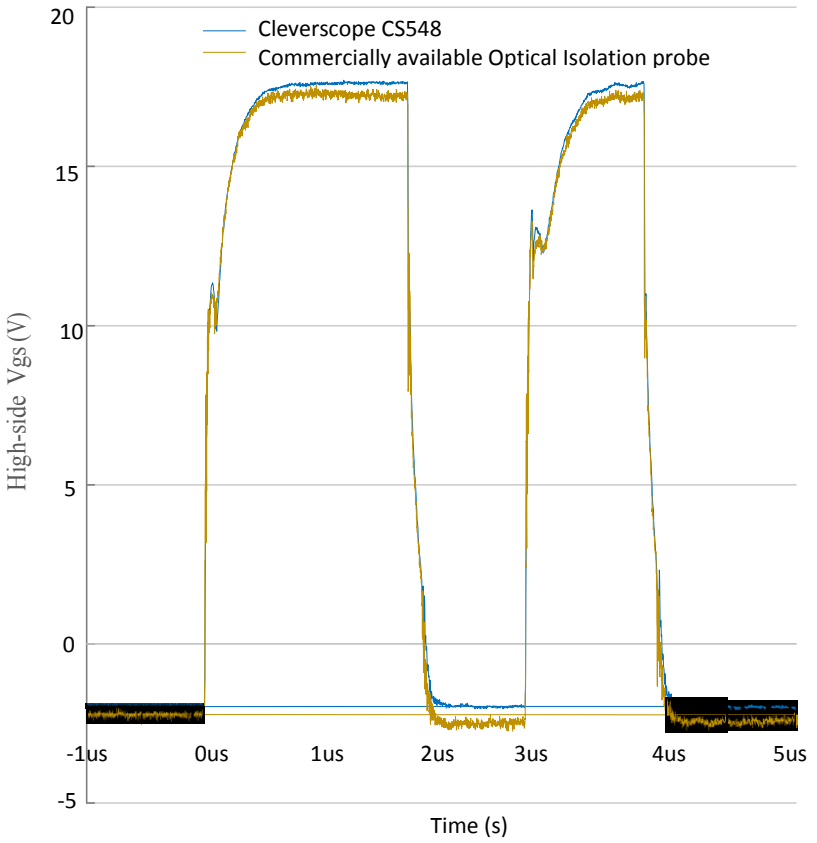
Where a feature has not been implemented yet, it includes an asterisk in the table above.

Selected Measurements

In this section we show some of the measurements that define the unique aspects of the CS548.

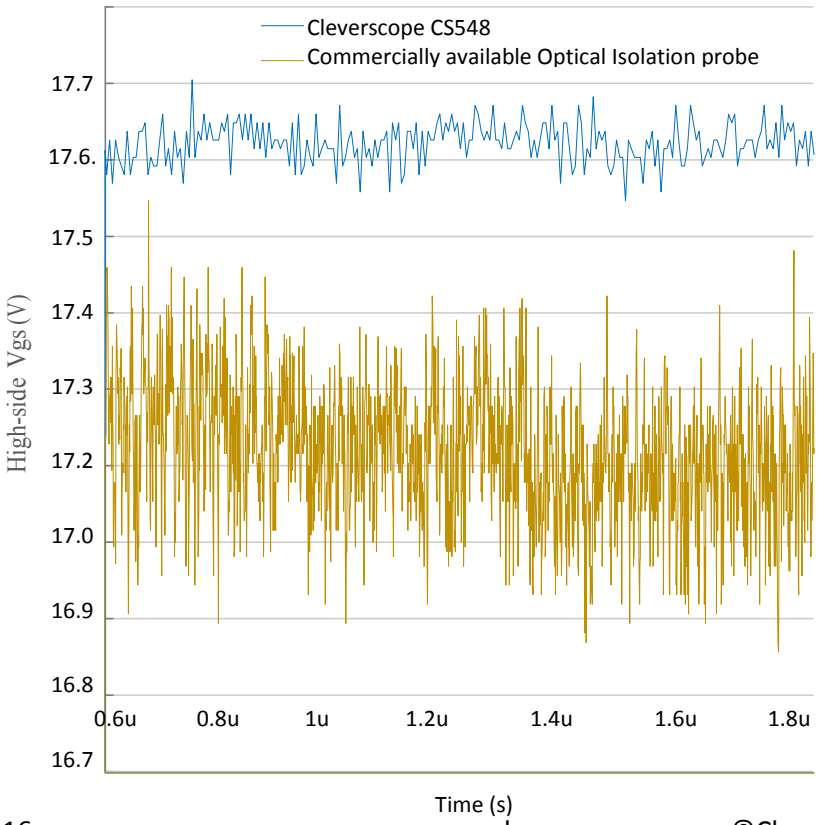
Below are comparison measurements between a Cleverscope CS548 and a commercially available Optical Isolation probe. These double pulse measurements were taken by a third party Oscilloscope manufacturer.

High Side Measurements of a Gate Drive



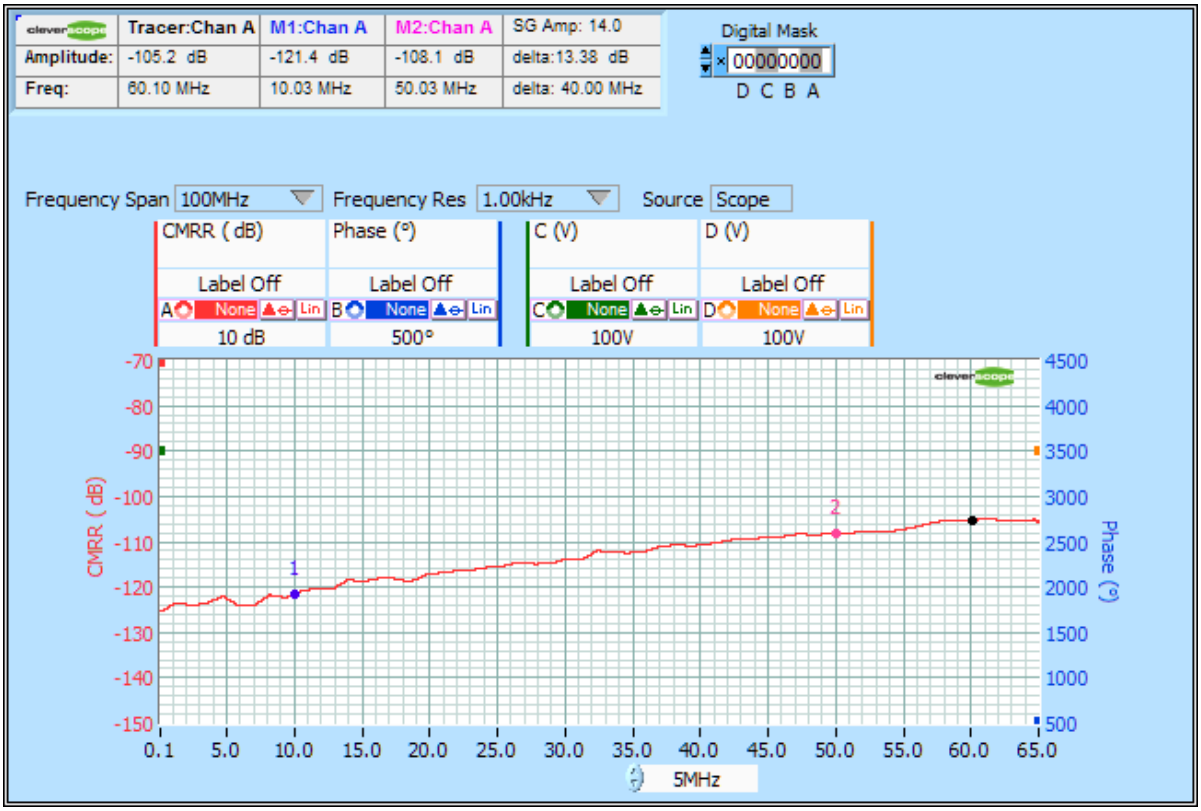
These graphs are showing the superior noise performance of the CS548 when compared with a commercially available optical isolation probe. The CS548 is using an 80V range to measure the 17V gate drive. The commercially available probe is using the most optimum voltage range and tip.

Note the increased noise of the commercially available Optical Isolation probe, expanded first pulse:



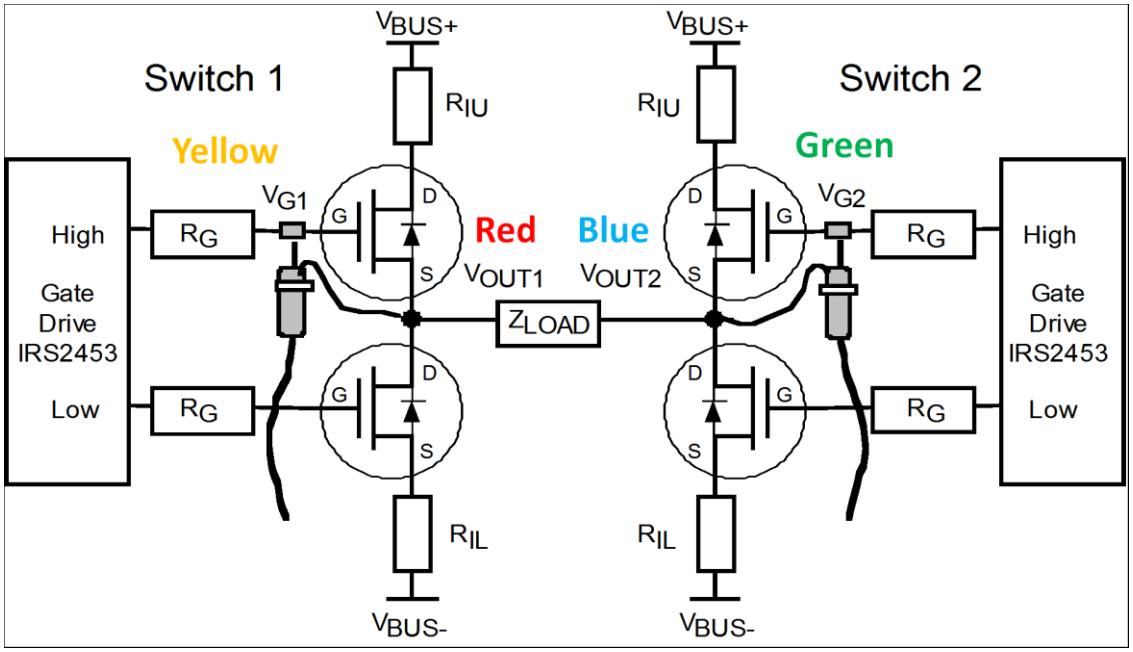
Common Mode Rejection

Typical channel CMRR is shown below:.

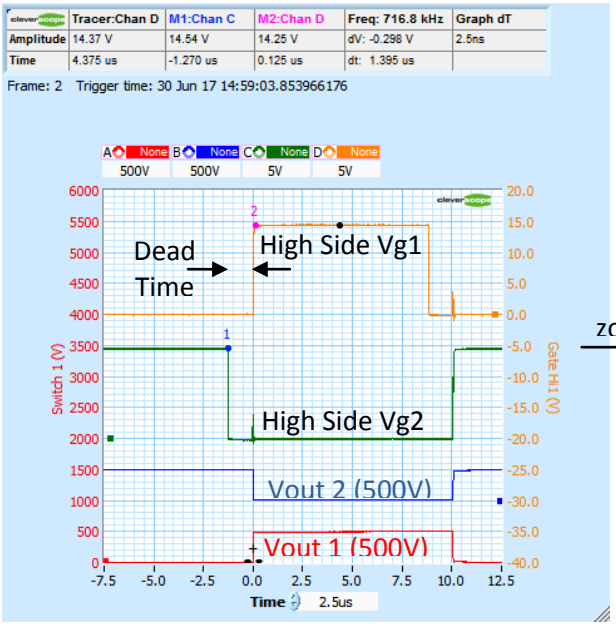


Application in switching Power Bridge

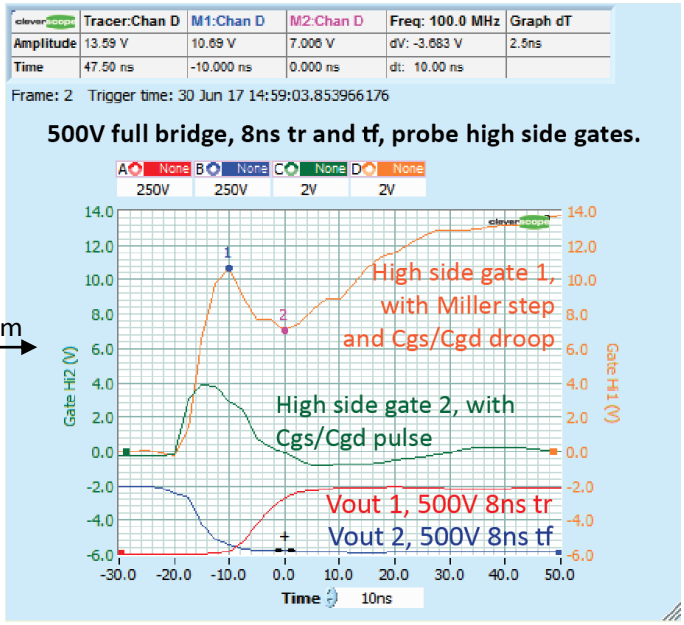
Using this full bridge setup, which swings 500V in 8ns:



We measure these results:



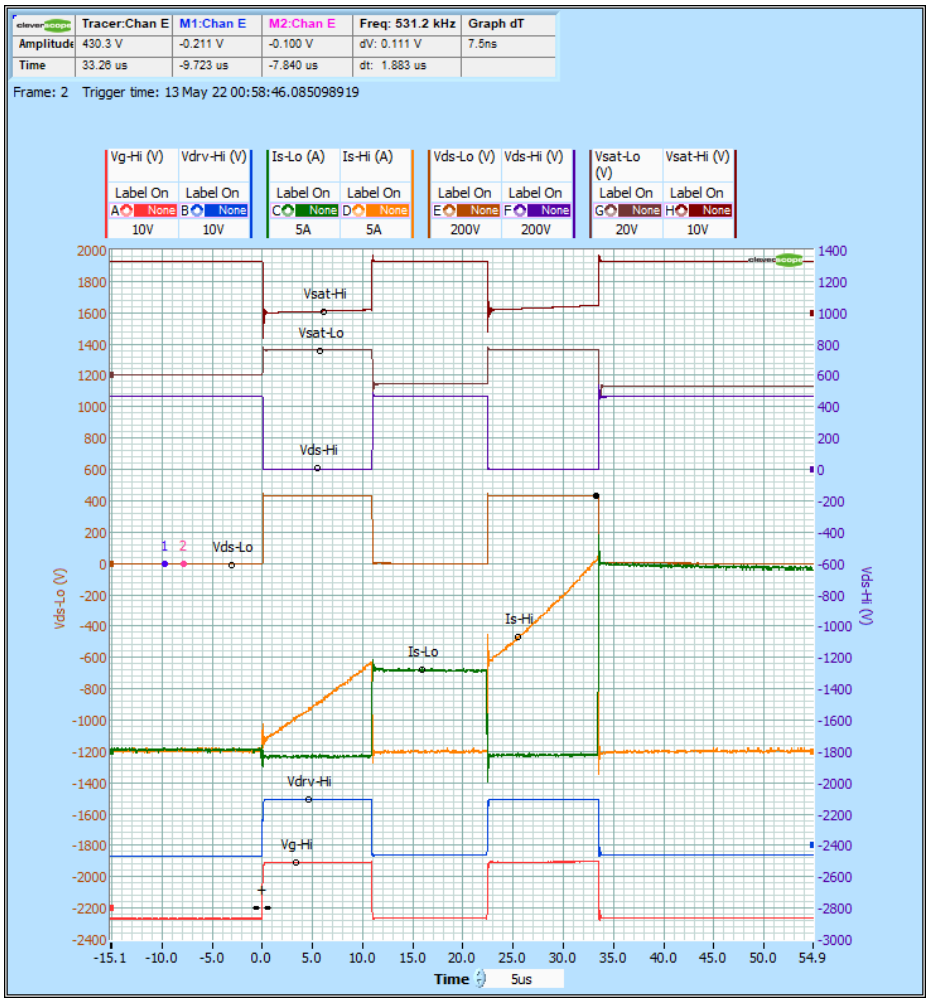
zoom



The high CMRR, and the isolation allow the high side gate drives to be measured without large common mode artifacts. We can observe dead time, pulse timing, the gate charge characteristic, and parasitics such as the Cgs/Cgd droop and pulse effects.

Measurements of a double pulse high side transistor with 8 channels

Two units can be slaved together using the Link Out port connected to the Link In port with the CS1021 500mm link cable. Here are two gates, two gate drives, and two Switch nodes on the full bridge:



Zoom in on the PDF to examine the detail.

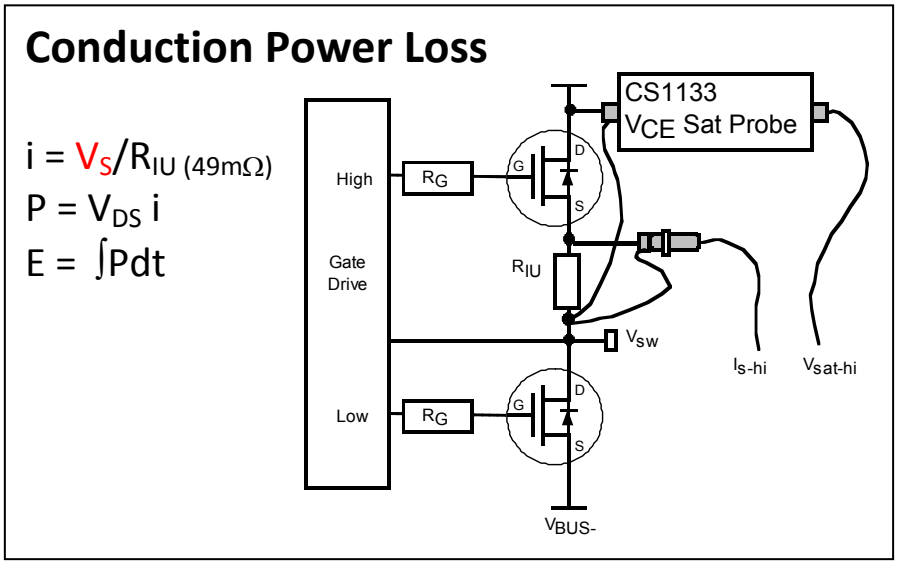
The current is rising in the load inductor during Pulse 1, we can examine the top transistor turn off and then turn on, and the rise in inductor current during Pulse 2. We can measure the conduction Power during the two pulses, and switching Power during turn off ad turn on.

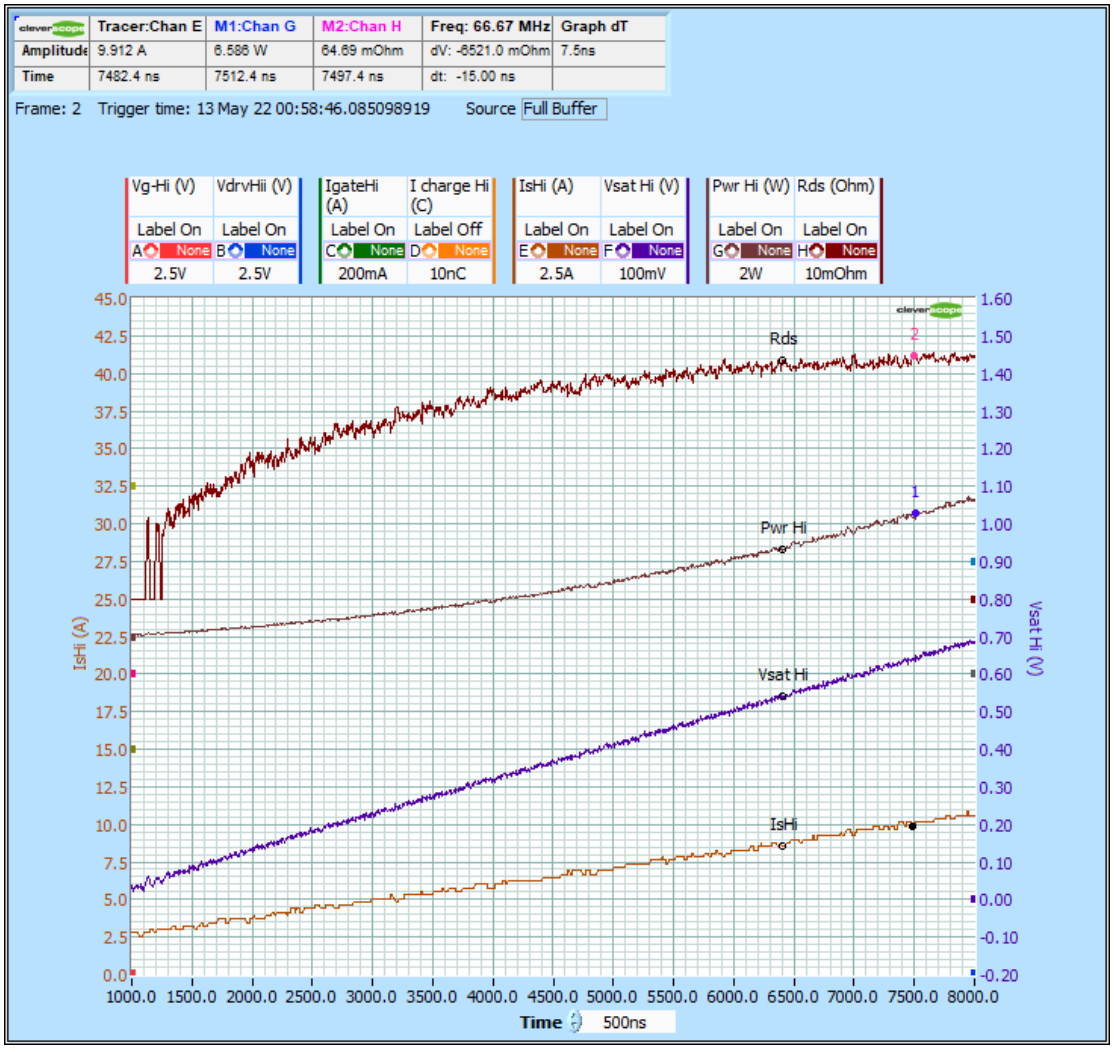
Channels are:

- Vsat Hi
- Vsat Lo
- Vds Hi
- Vds Lo
- Is hi
- Is lo
- Vdrv Hi
- Vg hi

Conduction Power

Using the Maths Graph we can calculate power Power and RDSON

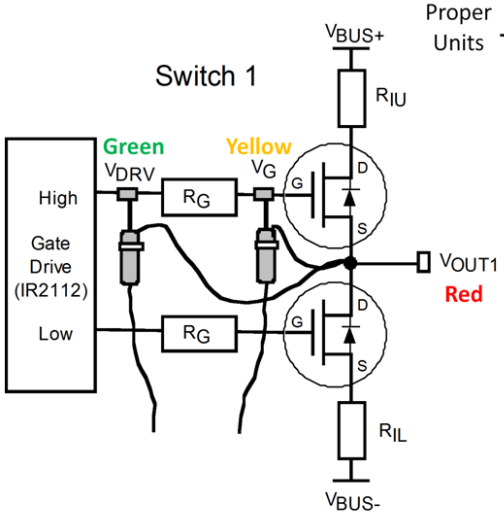




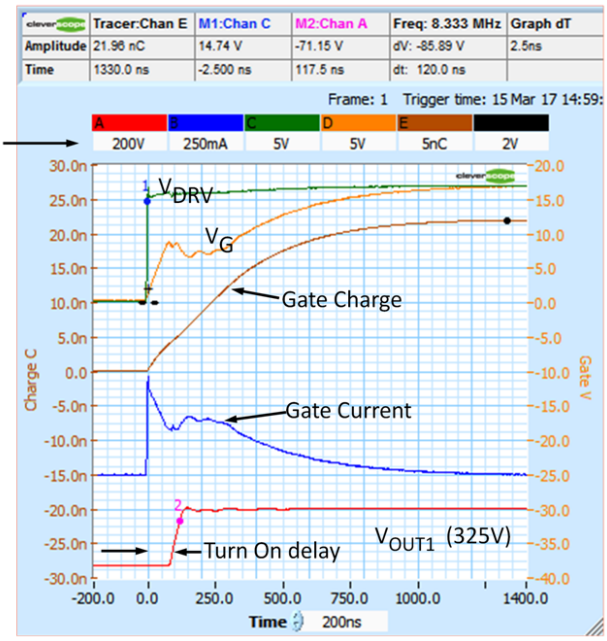
Using the Tracer on IsHi with a value of 9.912A, VsatHi is 542.8mV and Pwr Hi is 6.586W, with an RDS On of 64.69mOhm. (see the Tracer and Marker information at the top of the display).

Measuring Gate Charge in a SEW Movitrac Variable Speed Drive (VSD)

Measuring Gate Drive System
Example: SEW Movitrac



Proper Units →



Calculate Charge

$$Qg = \int Ig\ dt$$

Total Gate Charge
Qg = 22nC

Calculate Current

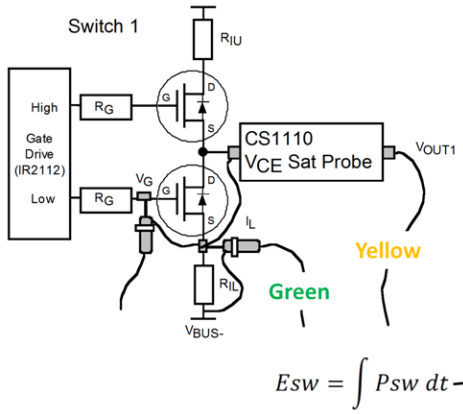
$$Ig = \frac{V_G - V_{DRV}}{RG}$$

Plateau gate current
Ig= 400mA

The high CMRR, and isolation allow making differential measurements across the gate drive resistor, even though it is swinging 325V in 37ns. Maths is used to calculate the gate current which is then integrated to calculate charge.

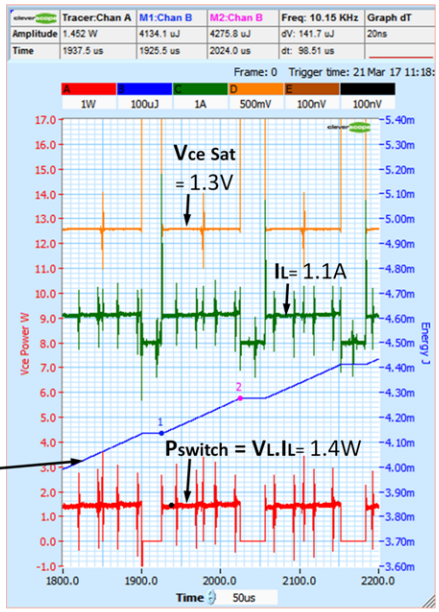
Measuring Conduction Power in a SEW Movitrac VSD

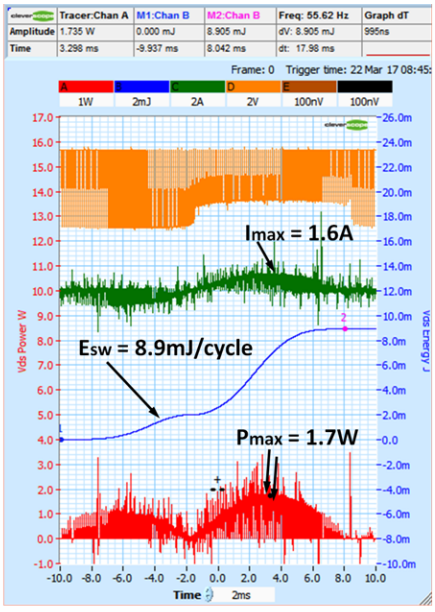
We use a Cleverscope V_{CE} Sat probe to accurately measure small voltages while exposed to large (<1000V) voltage swings.



$$Esw = \int Psw\ dt$$

Use a CS1110 VCE SAT probe to measure conduction peak, and averaged power loss.



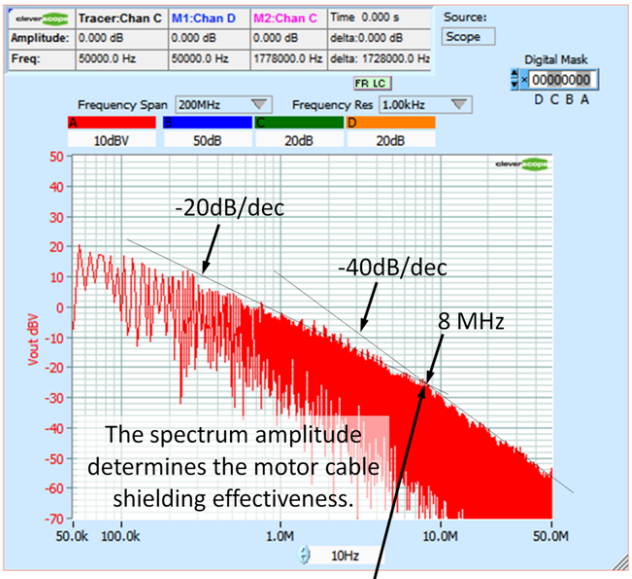


Esw/sec = 55 (Hz) x 8.9 = 494 mJ/s.
Average power = 494mW

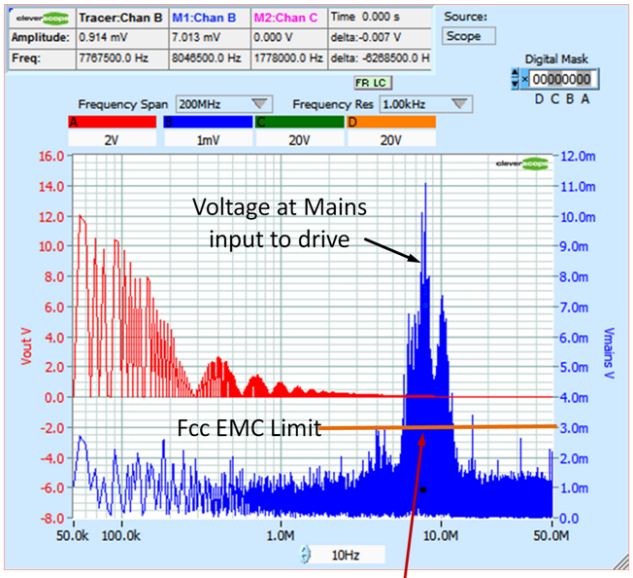
We use Maths to calculate the conduction current (green), the V_{CE} Sat probe to measure the switch saturation voltage (Yellow), the instantaneous power (red) and the energy per cycle (blue) to calculate the average conduction Power power (494 mW).

Measuring required shielding performance and EMC filtering effectiveness

We us 100x probes to measure the Switch voltage, and the input mains voltage safely.



The 20/40 dB/dec corner frequency is set by the rise time (F = 1/π 37ns). A slower rise time reduces how good the shield needs to be.

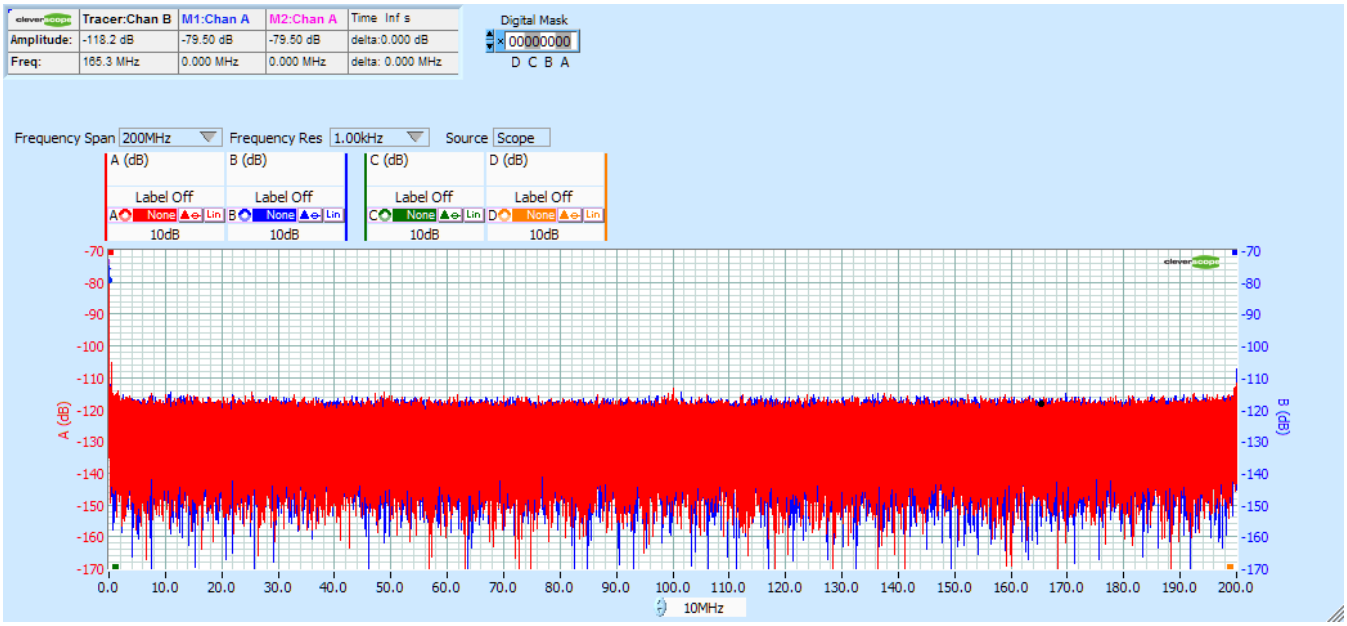


The mains input is not sufficiently filtered, and the drive does not meet the FCC standard. A slower rise time would help, and improved filtering.

This test uses the Spectrum Analyser.

Spectral Noise Floor

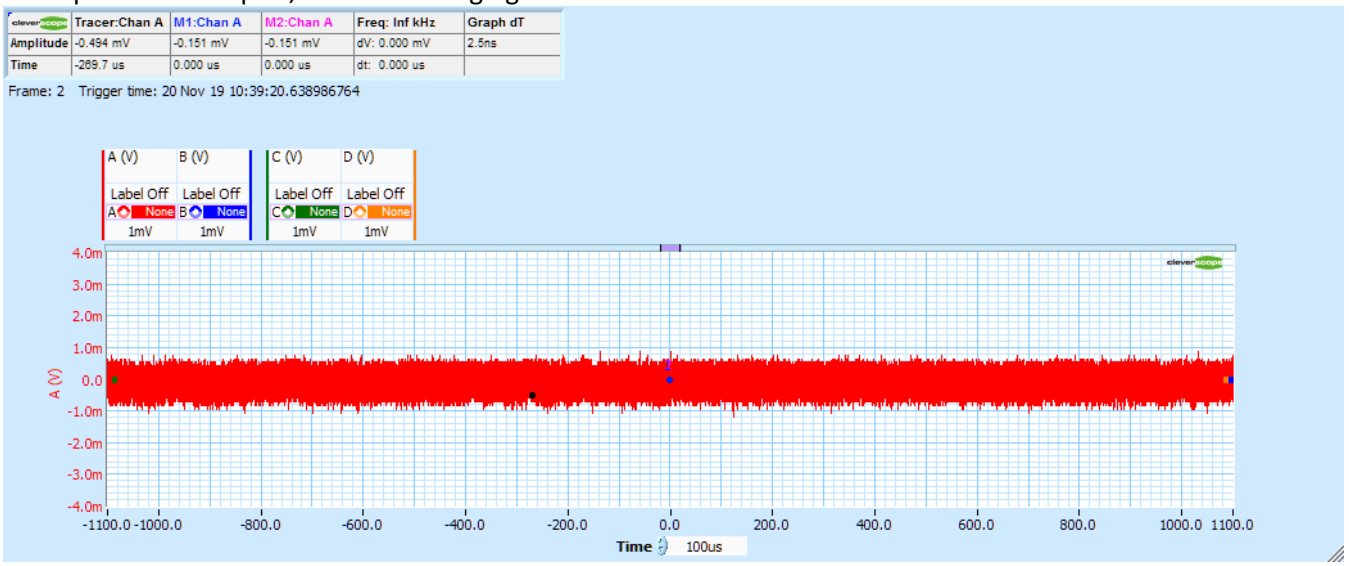
This is the full bandwidth noise with all four channels being captured with open inputs, 1kHz resolution, in dBV:



The noise floor is uniform, and below about -115 dBV per bin.

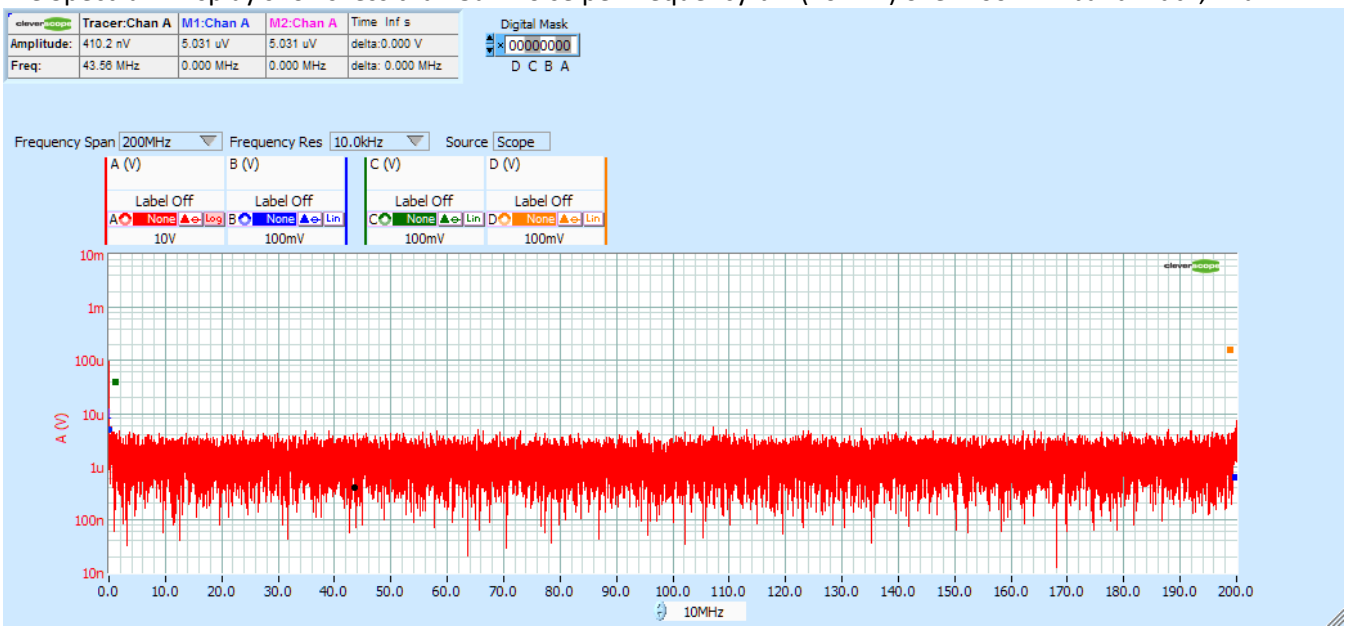
Time Noise Floor

We capture 1M samples, without averaging:

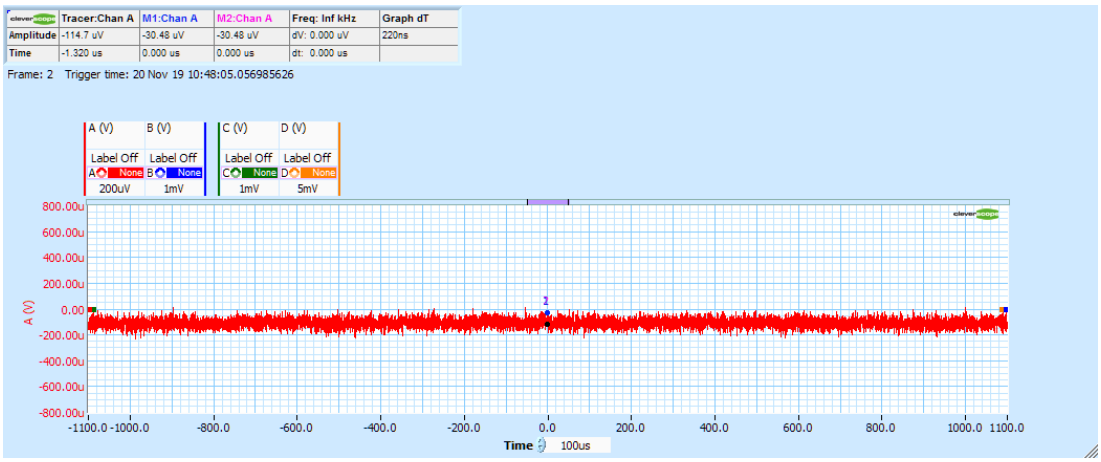


We use the signal information display to calculate the Standard Deviation (a good estimate of RMS, less the DC) and the peak to peak. We see about 200uVrms noise, and less than 1.8mV p-p noise.

The Spectrum Display shows less than 8uV noise per frequency bin (10 kHz) over 200MHz bandwidth, in uV:

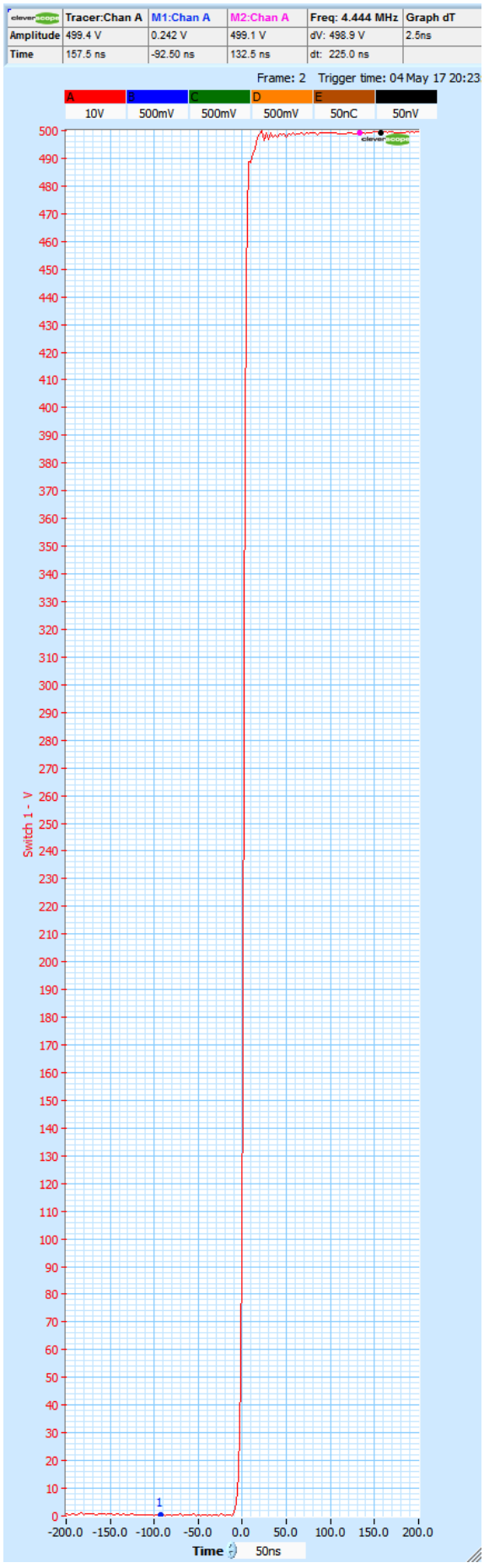


Averaging, and the moving average filter can be used to improve the noise floor to around 200uV p-p :

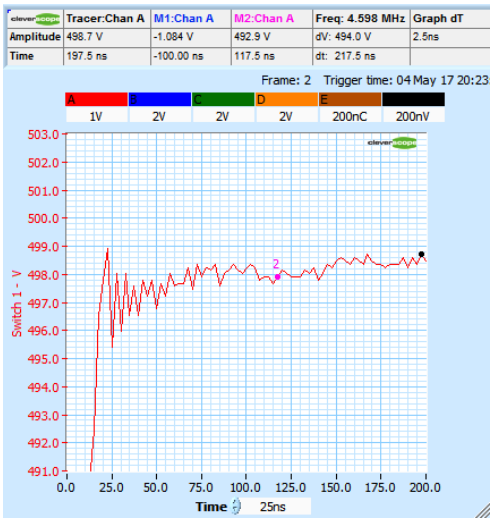


Response to 500V 10ns transition

We measure the CS1090 Switch 1 output (500V, 10ns rise time):



This trace shows the transition measured using a 100x probe. The display pixel resolution masks the actual channel resolution, shown here at 1V/div:

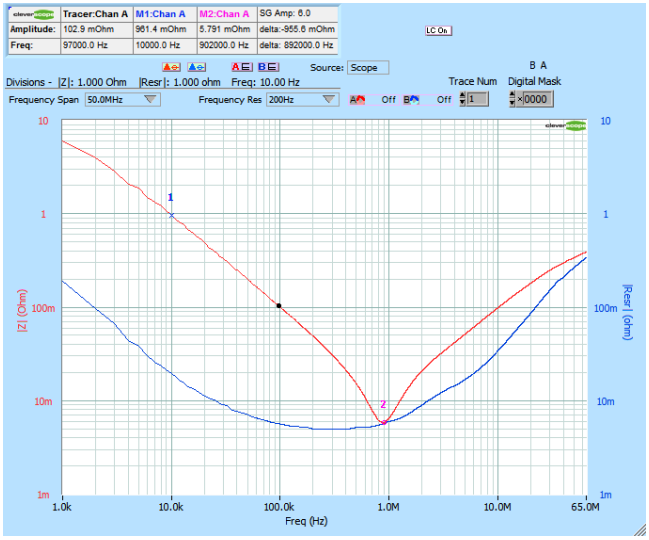


This kind of resolution is not possible with an 8 bit scope.

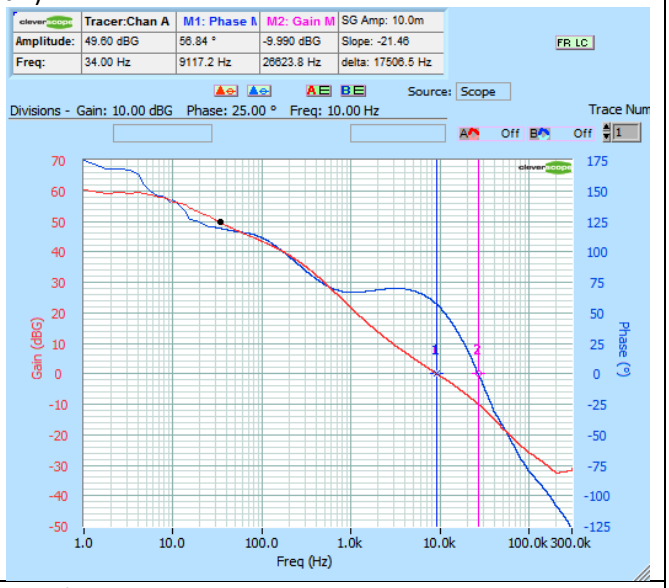
Frequency Response Analysis Functions (FRA)

The Frequency Response Analysis (FRA) system uses the isolated signal generator to provide stimulus for component, system or power supply measurements. The measurements available are shown in the Displays/FRA section of the data sheet. Here are a collection of measurements made using the FRA system (zoom on the PDF to see the detail):

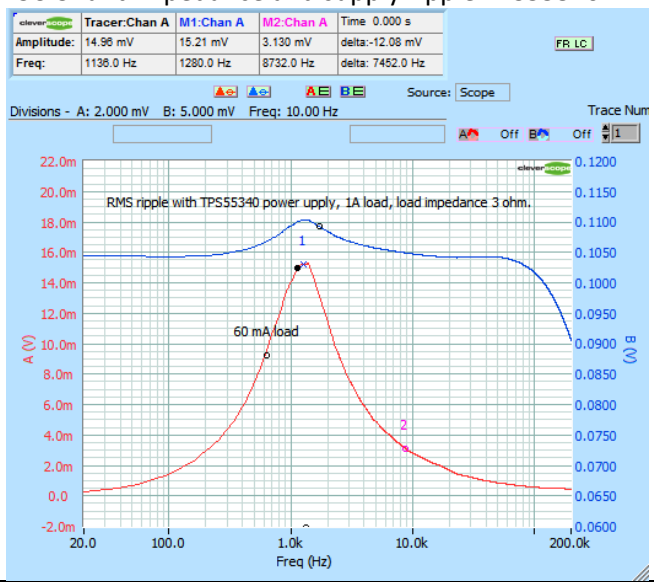
Impedance of a ceramic capacitor



PSU Gain Phase of switching power supply TPS55340 showing Phase Margin (56.8 deg) and Gain Margin (20 dB):



PSU Shunt Impedance and supply ripple TPS55340:



Gain/Phase of a 10.7 MHz filter:

TLV70433 PSRR using CS1070 (1A 50 MHz op-amp):

Powered LTC3589 Output Impedance using CS1070:

Cleverscope Application Specification

Calibration

Calibration method	Automatic self calibration
Calibration Voltage Source (Internal)	2.5V reference, 40 ppm stability (1000 Hrs) , 30 ppm/deg C
Calibration Voltage Source (external)	7.5V reference, 20 ppm stability, ±0.035% accuracy, 7 ppm/deg C using ISL21090-7.5

Displays

Windows	Simultaneous Capture, Tracking, Spectrum, Information, Maths, XY, Control Panel, Streaming, Frequency Response Analysis (FRA), Pulse Builder and Protocol setup windows
Scope window functions	Defines capture specification for signal acquisition unit, defining amount of time before trigger, amount of time after the trigger, lower amplitude limit, upper amplitude limit. Defines Tracking graph time position, when tracking graph is linked. Defines trigger level and direction Full zoom and Pan in both axis. Annotations. Custom units Custom colours
Tracking window functions	Displays zoomed section of captured signal. Resolution from 1ns to 5s/div. Full zoom and Pan in both axis. Annotations. Custom colours
Spectrum window functions	Display spectrum of signal captured in capture window. User definable resolution Full zoom and Pan in both axis. Annotations. Custom units Custom colours
Maths window function	Displays results of Maths equations. Maths equations are user entered expressions involving any of the inputs (analog and digital), previous maths equation line results, and an arbitrary number of function results (+ - * / sqrt, power, log, ln, all transcendental functions, equality functions). Custom units. Provide live Matlab link.
XY window function	Displays XY graph from source (Capture, tracking, spectrum, or Maths
Information window functions	Displays automated measurements (see below) Used to log derived information values to disk, with a period of between 0.05 – 86,400 secs per sample. Live logging to Excel DDE live value transfer to Excel.
Control window functions	Provides Trigger settings – analog and digital Provides Sample control – single, triggered or automatic. Provides access to tools – Pan, Zoom, Annotate Controls Frame store Controls Spectrum resolution, acquisition method and averaging
Frequency Response Analysis (FRA)	FRA control panel is used to setup up oscilloscope/signal generator to make automated measurements of these values vs frequency: • RMS Amplitude • Power • Power Density • Gain/Phase • Impedance + R_{ESR} or Q/D Factor or Phase • Capacitance + R_{ESR} or D Factor or Phase • Inductance + R_{ESR} or Q Factor or Phase • Shunt Impedance (magnitude without phase for low impedances) • PSU Gain/Phase - for finding Gain/Phase of powered up power supplies • PSU PSRR - for finding PSRR of powered up power supplies • PSU Output Impedance - for finding Output Impedance of powered up power supplies • PSU Input Impedance - for finding Input Impedance of powered up power supplies

	• Probe calibration functions for maximum accuracy.
Protocol Setup	Provides protocol setup for I2C, SPI , UART and parallel bus.
Pulse Builder	Allows manual control of isolated digital outputs state, Pulse Builder for pulse trains, PWM with up to 4 PWM generators, including single output, half bridge, or full bridge, and double pulse test for high side and low side.

Measurements

Cursors	Voltage Difference between cursors Time difference between cursors Reciprocal of ΔT in Hertz (1/ΔT).
Automated measurements	**Function**: DC, RMS, Max, Min, Pk-Pk, Std Dev, Period, Fundamental Frequency, Fundamental Peak amp, Pulse Length, Duty Cycle **Function**: 0 -> 1 Time, 1 -> 0 Time, V '1', V '0', V swing, Overshoot, Slew rate, Pulse Period, Pulse Frequency, Pulse Length, Duty Cycle **Function**: DC, RMS, Fsignal, Vsignal, F1, V1, F2, V2, F3, V3, SINAD, THD, HD2+3 **Function**: A at F, B at F, A max, A min, B max, B min, Amax at 0 B, Amin at 0 B, Bmax at 0 A, Bmin at 0 A, A -3dB L: H, B -3dB L: H
Custom units	6 characters
Custom signal names	20 characters
Custom scaling	Scale + offset by defining two (Vin,Vout) points
User definable colours	Signals, Background, Major Grid, Minor Grid

Mathematical Functions

Functions over the signal	Differentiation, Integration, Filtering, Power functions, Matlab interface, Signal Processing functions
Functions on a data point	Addition, subtraction, multiplication, division, squaring, square root, (inverse) sine, cosine, tangent, tangent, log, sign etc. Equality operations.
Maximum number of sequential mathematical equations	10, symbolic with multiple operators and operands.

Spectrum Analysis

Frequency Range	User definable, Range = 0- 1/Scope Graph ΔT Frequency axis – log or linear.
Analysis Output	RMS Amplitude, Power, Power Density, Gain/Phase
Frequency Resolution	In 1, 2, 2.5, 5 sequence with 1 part in 1M resolution.
Output type	Volts, Power, Gain/Phase in linear , dB, degree or radian values. Impedance, LCR, Q and DF. Custom units can be applied.
Window types	None, Hanning, Hamming, Blackman-Harris, Flat top, Low Sidelobe
Averaging	Moving average, block average, peak hold.
Averaging method	Vector averaging in time domain if triggered. RMS averaging in frequency domain if not triggered.

Protocol Decode

Protocols	I2C, SPI , UART and parallel bus.
Protocol decode inputs	Digital Inputs 1-8, External trigger, Channels A, B User defined threshold when using analog inputs
Protocol decode variables	Number of bits, Clock edge rising or falling, Bit invert/non Invert, Select Hi/Lo, MSB first or not, Number of stop bits.
Output display type	Naming label. Character, Hexadecimal or Decimal Number. Colour.

Streaming

Sampling Rate	12 SPS – 3 MSPS (Streaming rate will be improved in the future)
Sample preparation	Peak capture or Filter prior to decimation. Using 10MHz filter with 14 bit ADC we achieve 13 bits ENOB at 3 MSPS (60uV noise floor with +/-0.8V range).
Sample storage	Up to 500 G samples. Samples are stored in multiple smaller files to increase speed.
Review capabilities	Zoom and pan anywhere in sample space. Samples are displayed peak captured (ie 1us pulse will still be visible in 1 day long sample record).
Export capabilities	Export tab delimited text, binary, or cleverscope format file. Output between markers, or current display. Set output depth.

Data Export

File types output	Cleverscope proprietary, Tab delimited text (Excel compatible), Excel file (for signal information logging), binary (format given in help).
Live Data output	DDE to Exel, direct placement of data into live Excel sheet Live data output to and return from Matlab

Windows facilities

Standard Functions	Copy and Paste Save and Open native format (saves full setup) Save and Open tab delimited text file Save and Open binary file (start time, dt, data) Print with Date/Time, File Name and Description. Print Setup
Windows	Dynamically resized Can be placed anywhere on desktop Can be docked to move with Cleverscope Control Panel Can be docked to minimize/restore with one click.
User defined units	6 characters
User defined signal names	20 characters
User defined scaling	Scale + offset by defining two (Vin,Vout) points
User definable colours	Signals, Background, Major Grid, Minor Grid

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Document changes:

5 May 2017 v1.1 - Original
12 July 2018 v1.2 - Added Specification Status section.
20 Nov 2019 v1.3 - Added 8 channel display
16 May 2022 v1.0 - for CS548 specification.
8 July 2022 v1.2 - Addition of CS1133 and CS1233. Minor changes to CS548 Specification.
10 Feb 2023 v1.3 - CS5X8 Options
22 Feb 2023 v1.4 -Added other system items and new photos
18 Aug 2023 v1.5 - Add ‘Warning’ section.

